

General Description

The MY5N10C uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

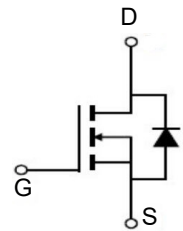
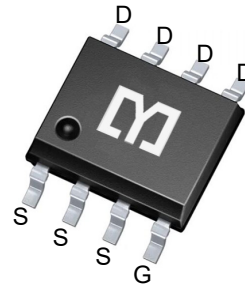


Features

V_{DSS}	100	V
I_D	5	A
$P_D(T_A=25^{\circ}C)$	17	W
$R_{DS(ON)}(at V_{GS}=4.5V)$	<140	m Ω

Application

- Battery protection
- Load switch
- Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY5N10C	SOP-8	140INC	3000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^{\circ}C$	I_D	5	A
Pulsed drain current ²⁾ , $T_C=25^{\circ}C$	$I_{D, pulse}$	15	A
Power dissipation ³⁾ , $T_C=25^{\circ}C$	P_D	17	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	1.2	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	$^{\circ}C$
Thermal resistance, junction-case	$R_{\theta JC}$	7.4	$^{\circ}C/W$
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	62	$^{\circ}C/W$

Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-source breakdown voltage	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	100			V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$	1.2	1.5	2.5	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS}=10\text{ V}$, $I_D=5\text{ A}$		110	140	$\text{m}\Omega$
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS}=4.5\text{ V}$, $I_D=3\text{ A}$		160	180	$\text{m}\Omega$
I_{GSS}	Gate-source leakage current	$V_{GS}=20\text{ V}$			100	nA
		$V_{GS}=-20\text{ V}$			-100	
I_{DSS}	Drain-source leakage current	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$			1	μA
C_{iss}	Input capacitance	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=100\text{ kHz}$		206.1		pF
C_{oss}	Output capacitance			28.9		pF
C_{rss}	Reverse transfer capacitance			1.4		pF
$t_{d(on)}$	Turn-on delay time	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_G=2\text{ }\Omega$, $I_D=5\text{ A}$		14.7		ns
t_r	Rise time			3.5		ns
$t_{d(off)}$	Turn-off delay time			20.9		ns
t_f	Fall time			2.7		ns
Q_g	Total gate charge	$I_D=5\text{ A}$, $V_{DS}=50\text{ V}$, $V_{GS}=10\text{ V}$		4.3		nC
Q_{gs}	Gate-source charge			1.5		nC
Q_{gd}	Gate-drain charge			1.1		nC
$V_{plateau}$	Gate plateau voltage			5.0		V
I_S	Diode forward current	$V_{GS}<V_{th}$			7	A
I_{SP}	Pulsed source current				21	
V_{SD}	Diode forward voltage	$I_S=7\text{ A}$, $V_{GS}=0\text{ V}$			1.0	V
t_{rr}	Reverse recovery time	$I_S=5\text{ A}$, $di/dt=100$ $\text{A}/\mu\text{s}$		32.1		ns
Q_{rr}	Reverse recovery charge			39.4		nC
I_{rrm}	Peak reverse recovery current			2.1		A

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^{\circ}\text{C}$.
- 5) $V_{DD}=50\text{ V}$, $R_G=50\text{ }\Omega$, $L=0.3\text{ mH}$, starting $T_J=25\text{ }^{\circ}\text{C}$.

Typical Characteristics

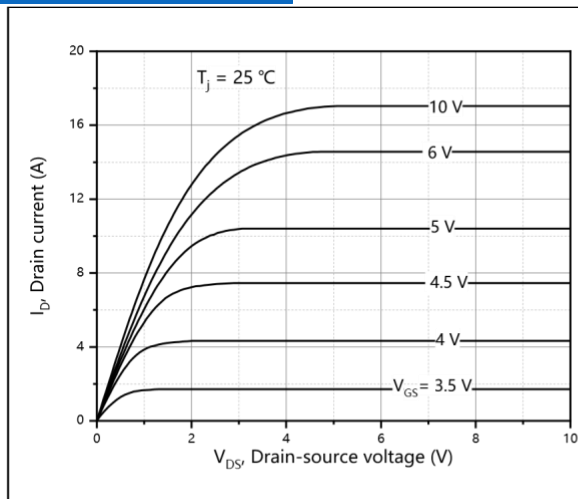


Figure 1, Typ. output characteristics

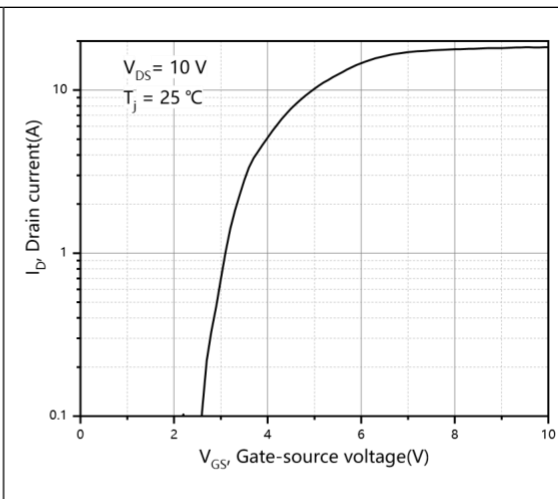


Figure 2, Typ. transfer characteristics

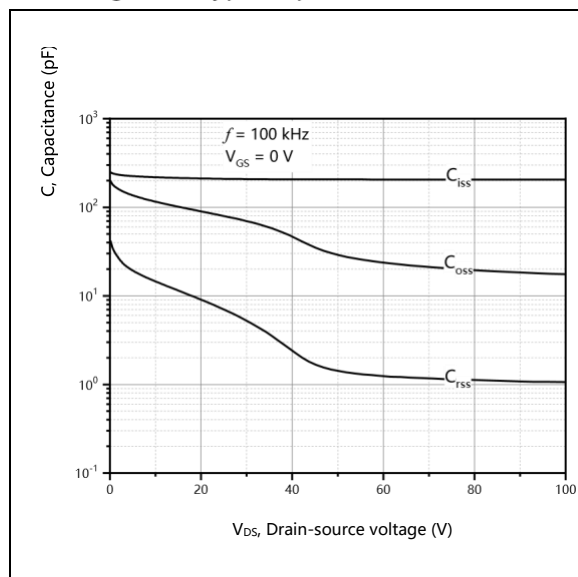


Figure 3, Typ. capacitances

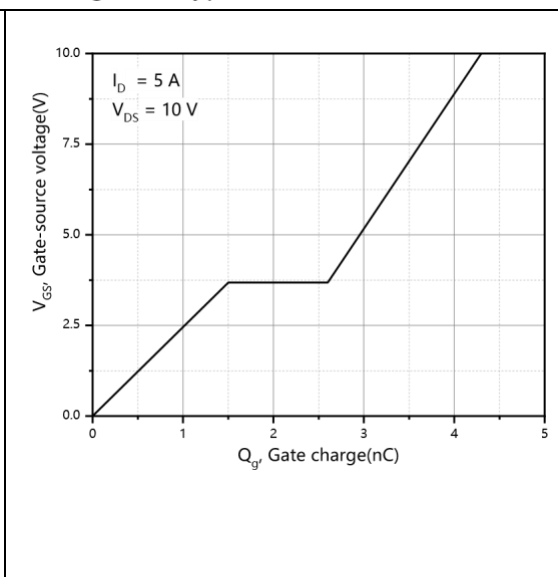


Figure 4, Typ. gate charge

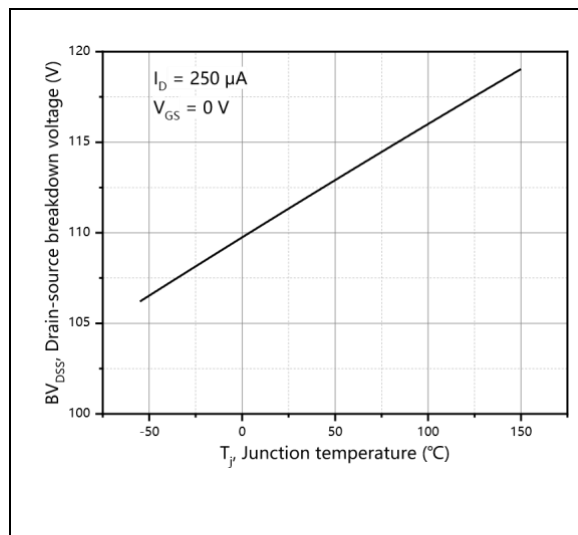


Figure 5, Drain-source breakdown voltage

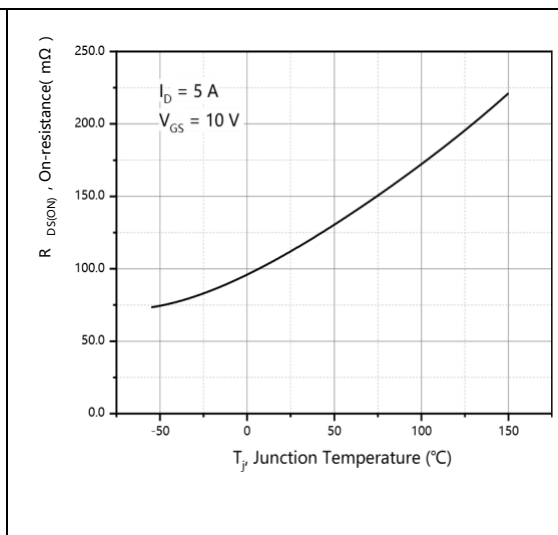


Figure 6, Drain-source on-state resistance

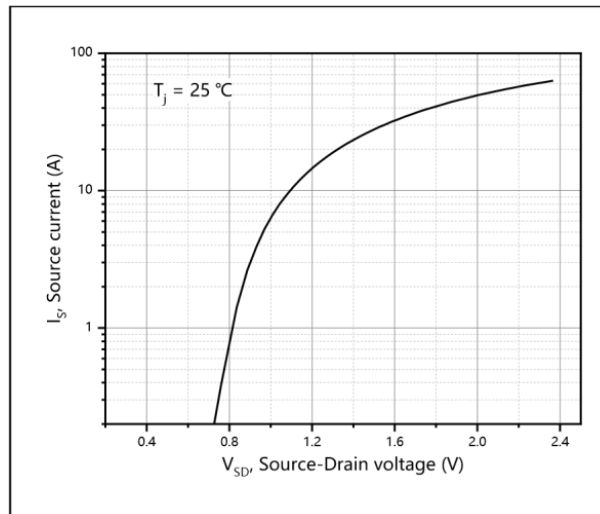


Figure 7, Forward characteristic of body diode

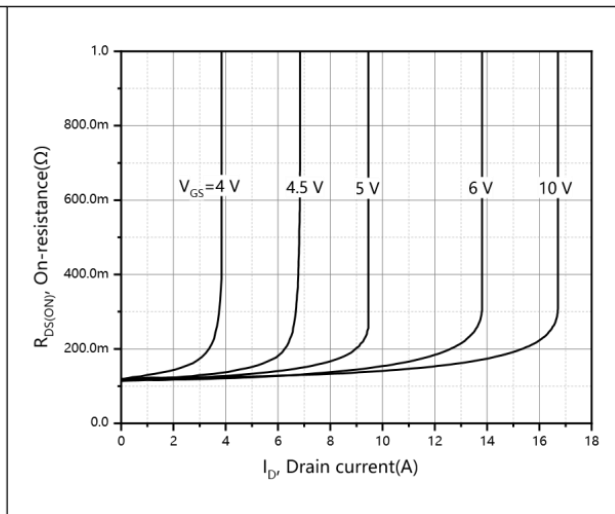


Figure 8, Drain-source on-state resistance

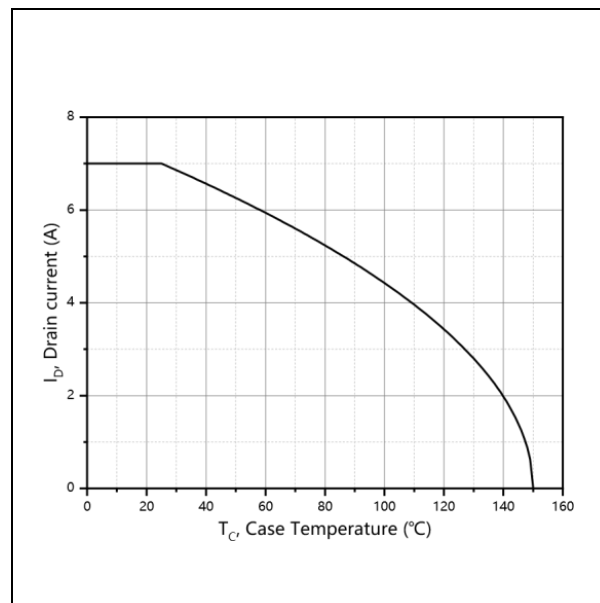


Figure 9, Drain current

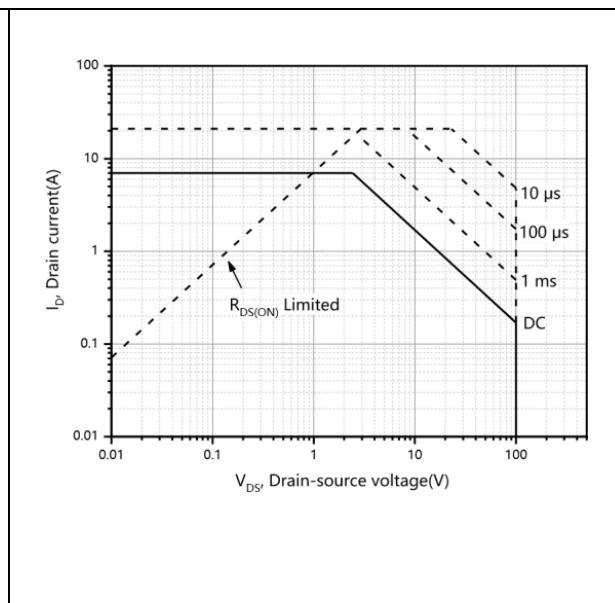


Figure 10, Safe operation area $T_C=25\text{ }^{\circ}\text{C}$

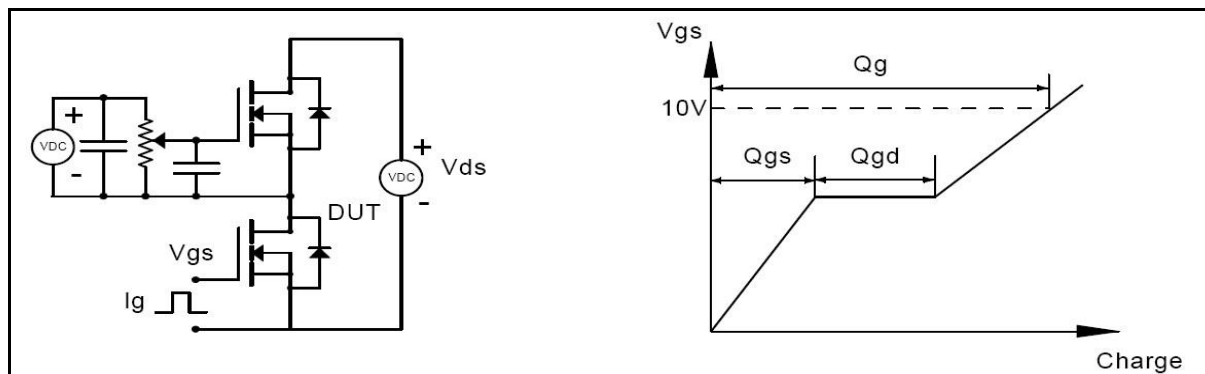


Figure 1, Gate charge test circuit & waveform

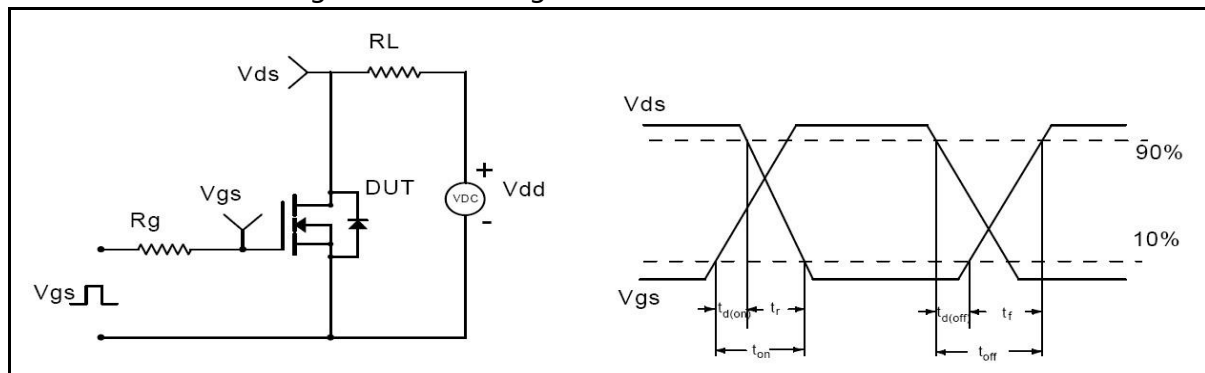


Figure 2, Switching time test circuit & waveforms

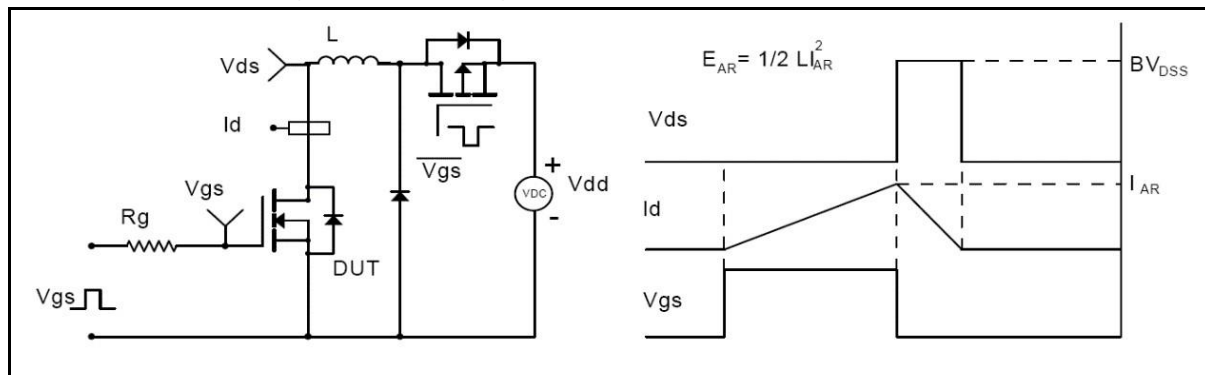


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

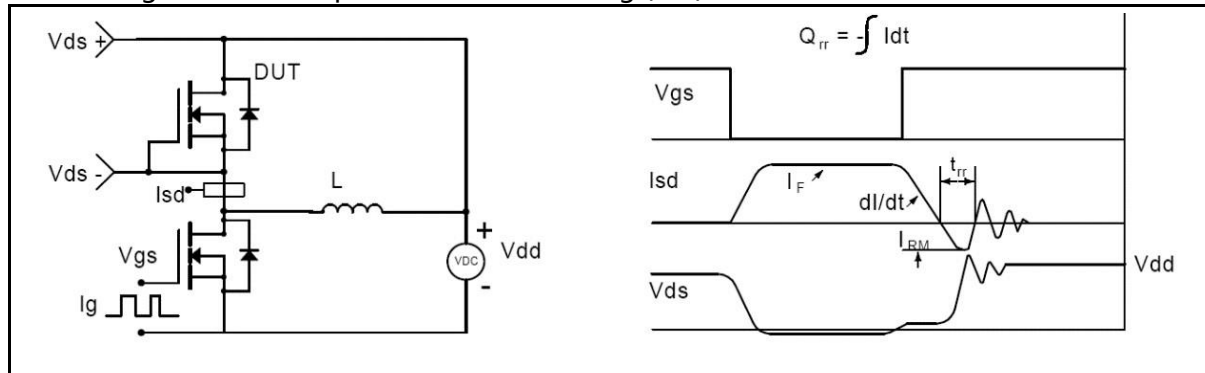
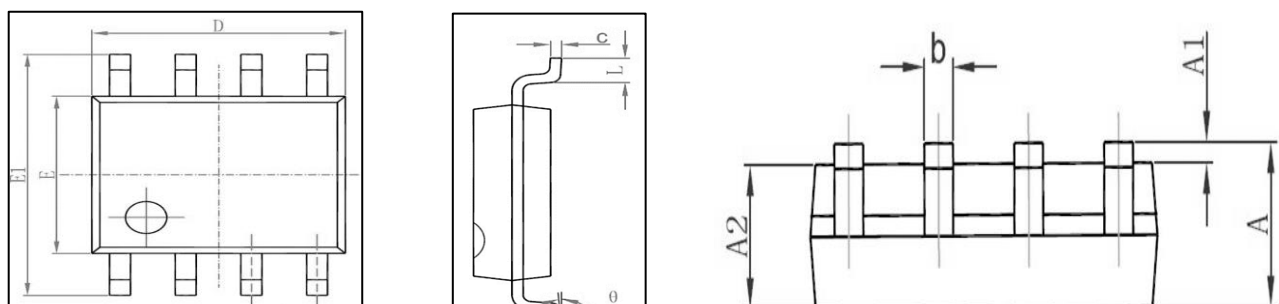
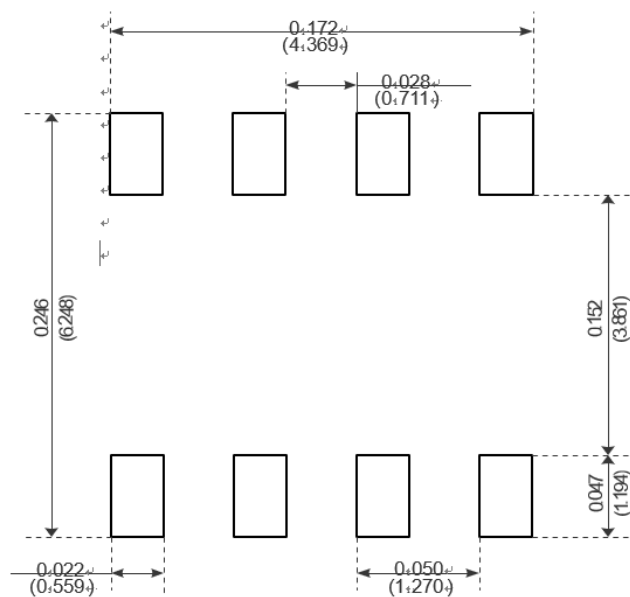


Figure 4, Diode reverse recovery test circuit & waveforms

Package Mechanical Data-SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads