

General Description

The MY30P03NE3 is the single P-Channel logic enhancement mode power field effect transistors to provide excellent $R_{DS(on)}$, low gate charge and low gate resistance.

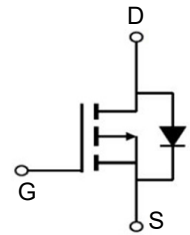
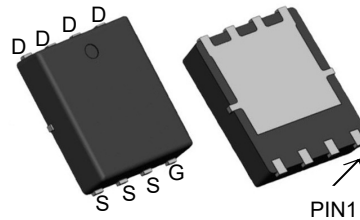


Features

V_{DSS}	-30	V
I_D	-30	A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	17	m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	25	m Ω

Application

- Battery protection System
- Switching power supply, SMPS
- DC/DC Converter
- DC/AC Converter
- Load Switch



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY30P03NE3	PDFN3*3-8L	MY30P03NE3	5000

Absolute Maximum Ratings ($T_J=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-30	V
VGS	Gate-Source Voltage	+20	V
$I_D@T_A=25^{\circ}C$	Drain Current ³ , V_{GS} @ 10V	-30	A
$I_D@T_A=70^{\circ}C$	Drain Current ³ , V_{GS} @ 10V	-23	A
IDM	Pulsed Drain Current ¹	-80	A
$P_D@T_A=25^{\circ}C$	Total Power Dissipation	3.57	W
TSTG	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$
Rthj-c	Maximum Thermal Resistance, Junction- case	6	$^{\circ}C/W$
Rthj-a	Maximum Thermal Resistance, Junction- ambient ³	35	$^{\circ}C/W$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain- Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =- 10V, I _D =-20A	-	17	22	mΩ
		V _{GS} =-4.5V, I _D =- 10A	-	25	32	mΩ
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1.0	-1.6	-2.5	V
g _{fs}	Forward Transconductance	V _{DS} =- 10V, I _D =-6A	-	15	-	S
IDSS	Drain- Source Leakage Current	V _{DS} =-30V, V _{GS} =0V	-	-	-1	uA
IGSS	Gate- Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =-6A	-	15	24	nC
Q _{gs}	Gate- Source Charge	V _{DS} =- 15V	-	3	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-4.5V	-	8	-	nC
td(on)	Turn-on Delay Time	V _{DS} =- 15V	-	12	-	ns
t _r	Rise Time	I _D =- 1A R _G =3.3Ω	-	7.5	-	ns
td(off)	Turn-off Delay Time	V _{GS} =- 10V	-	39	-	ns
t _f	Fall Time		-	21	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1260	2000	pF
C _{oss}	Output Capacitance	V _{DS} =- 15V f=1.0MHz	-	245	-	pF
C _{rss}	Reverse Transfer Capacitance	I _S =-6A, V _{GS} =0V, dI/dt=100A/μs	-	210	-	pF
trr	Reverse Recovery Time		-	19	-	ns
Q _{rr}	Reverse Recovery Charge		-	10	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test

Typical Characteristics

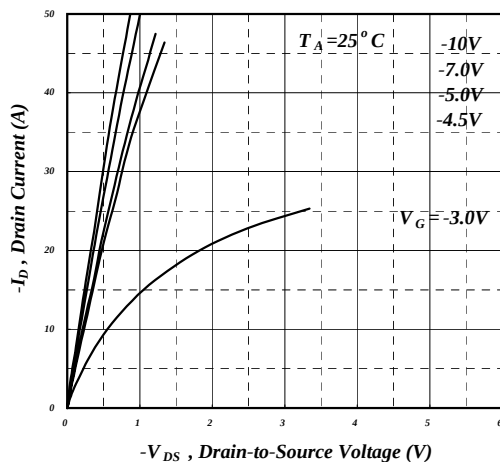


Fig 1. Typical Output Characteristics

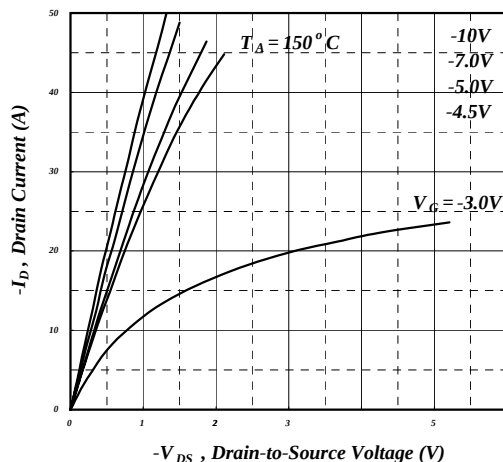


Fig 2. Typical Output Characteristics

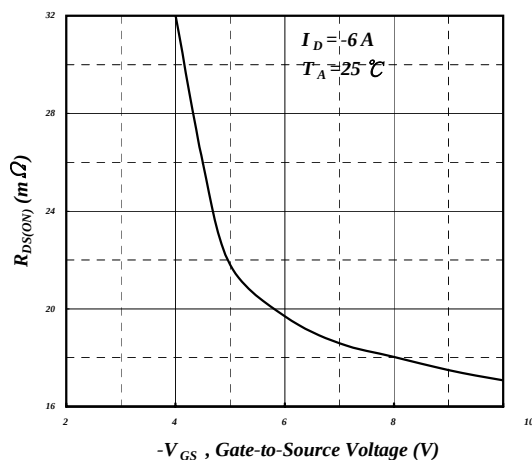
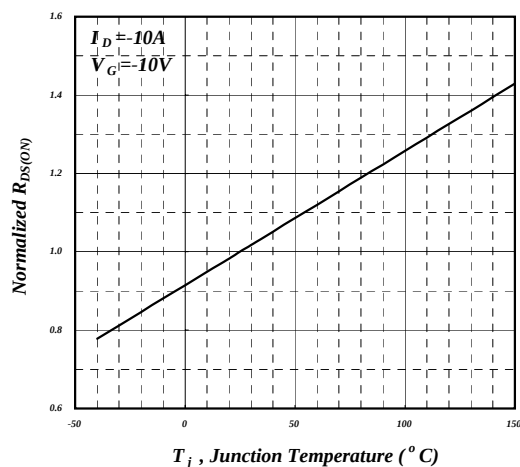
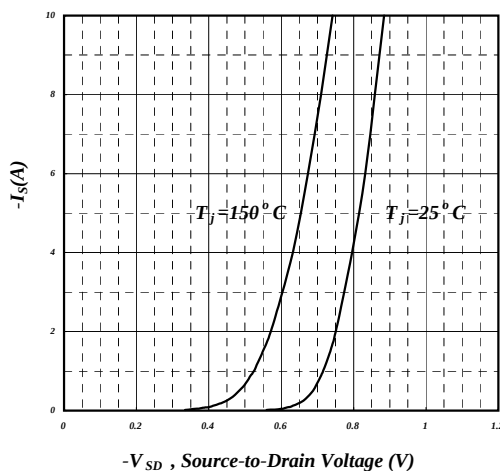


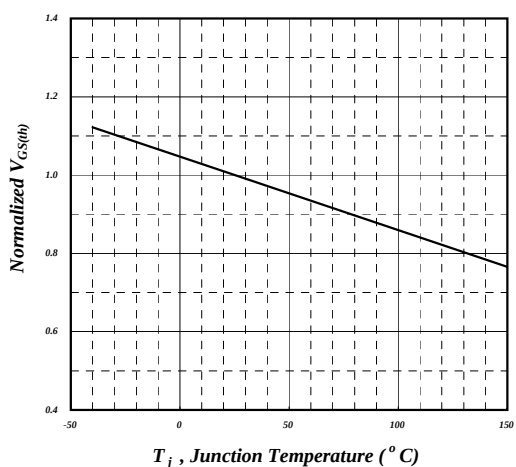
Fig 3. On-Resistance v.s. Gate Voltage



**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**



**Fig 5. Forward Characteristic of
Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s.
Junction Temperature**

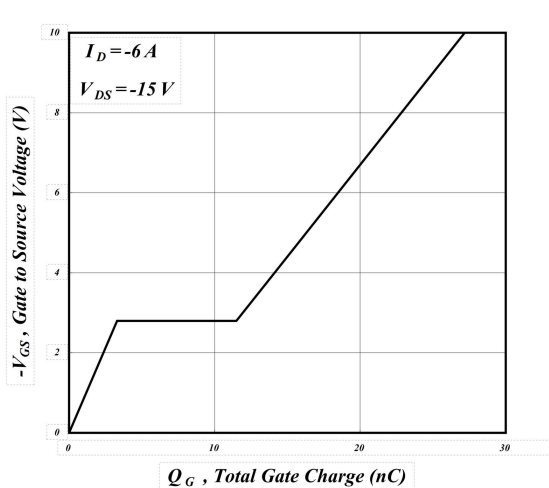


Fig 7. Gate Charge Characteristics

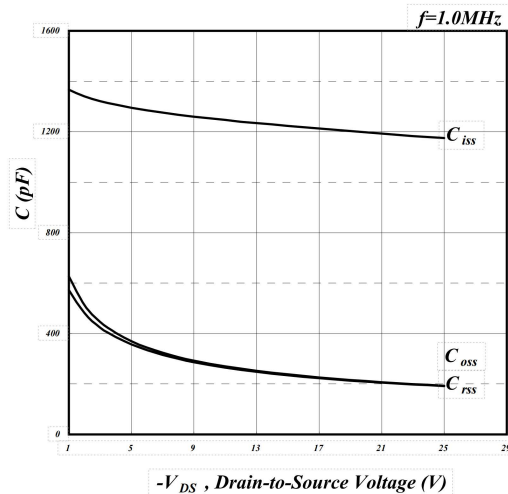


Fig 8. Typical Capacitance Characteristics

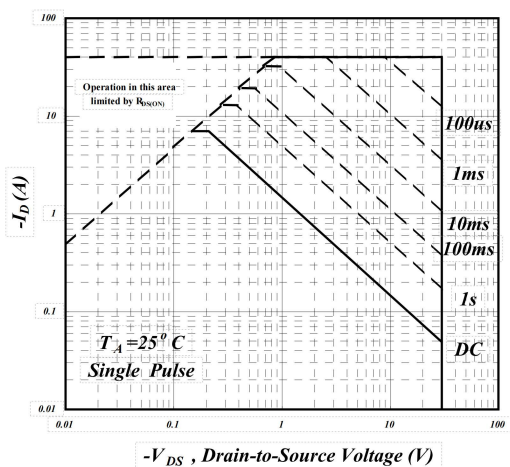


Fig 9. Maximum Safe Operating Area

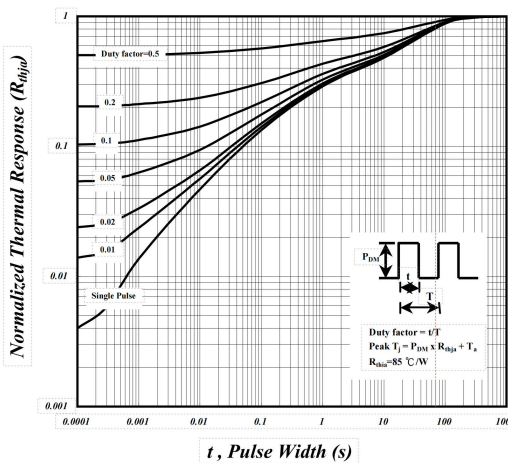


Fig 10. Effective Transient Thermal Impedance

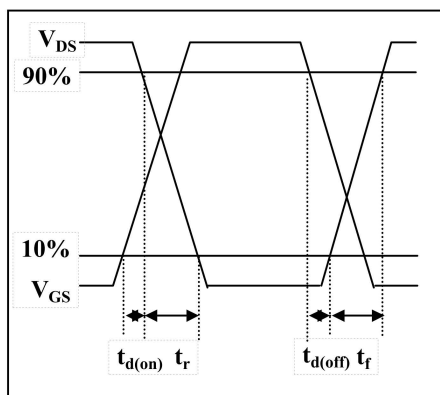


Fig 11. Switching Time Waveform

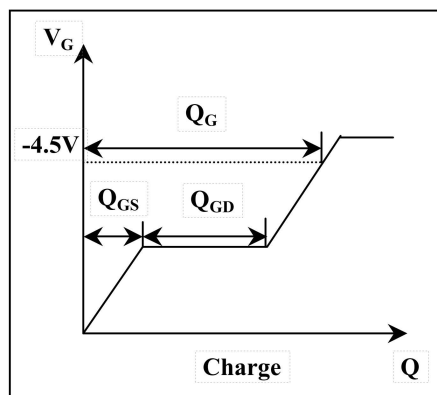
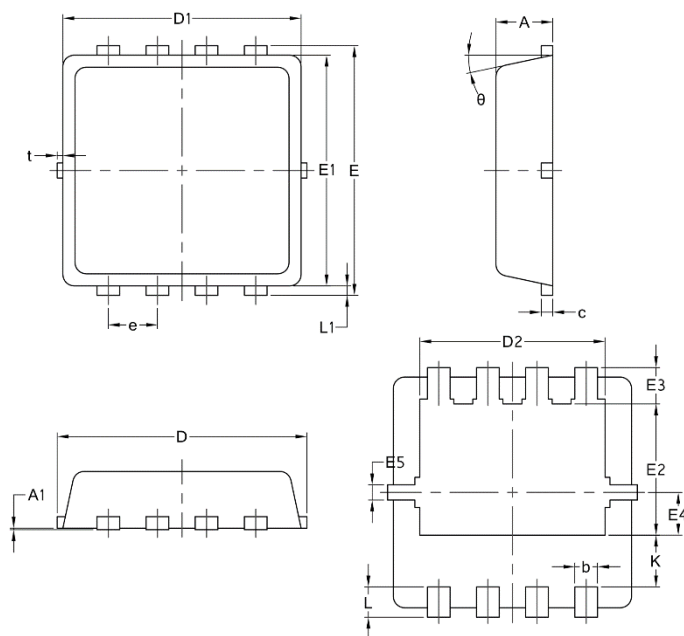


Fig 12. Gate Charge Waveform

Package Mechanical Data-DFN3*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14